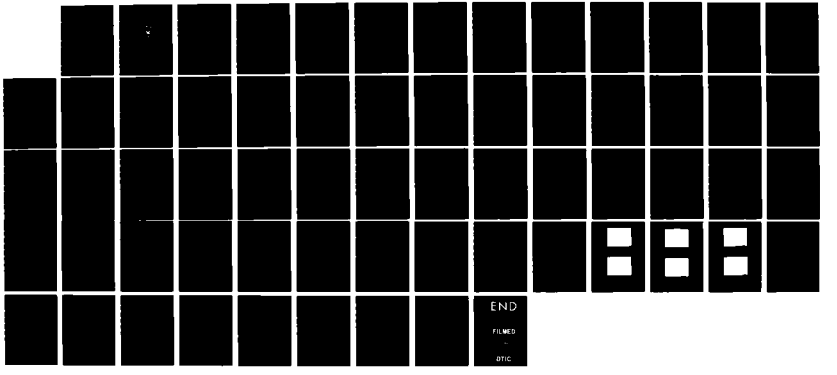
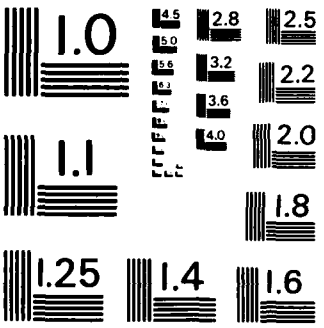
AD-A161 394 LOW-NOISE PHASE/FREQUENCY DETECTOR(U) NAVAL POSTGRADUATE SCHOOL MONTEREY CA J W MCCORKLE SEP 85 1/1

UNCLASSIFIED F/G 9/5 NL





NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

LOW-NOISE PHASE/FREQUENCY DETECTOR

by

John William McCorkle

September 1985

Thesis Advisor: G. A. Myers

Approved for public release; distribution unlimited

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A161394
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) Low-Noise Digital Phase/Frequency Detector	5. TYPE OF REPORT & PERIOD COVERED Master's Thesis September 1985
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) John William McCorkle	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Postgraduate School Monterey, California 93943-5100	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Postgraduate School Monterey, California 93943-5100	12. REPORT DATE September 1985
	13. NUMBER OF PAGES 61
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report)
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Phase Detector,
Phase-Locked-Loop,
Coherent Oscillator

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The purpose of the research reported on in this paper, is to demonstrate the effectiveness of a new circuit technique proposed by the author to eliminate the dead-zone anomaly in a digital phase/frequency detector. In addition to demonstrating the elimination of the dead zone, a new loop filter is described. The filter takes advantage of the new phase detector circuit technique so as to simultaneously provide both low-level reference sidebands and a lock-up time of one cycle of the reference.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

S N 0102-LF-014-6601

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

Approved for public release; distribution unlimited.

Low-Noise Digital Phase/Frequency Detector

by

John W. McCorkle
Electronics Engineer, Naval Surface Weapons Center
B.S.E.E.,
Virginia Polytechnic Institute and State University, 1975

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
September 1985

Author: John W. McCorkle
John William McCorkle

Approved by: Glen A. Myers
Glen Myers, Thesis Advisor

Gerald Ewing
Gerald Ewing, Second Reader

Harriett Rigas, Chairman,
Department of Electrical and Computer Engineering

John Dyer
John Dyer, Dean of Science and Engineering

ABSTRACT

The purpose of the research reported on in this paper, is to demonstrate the effectiveness of a new circuit technique proposed by the author to eliminate the dead-zone anomaly in a digital phase/frequency detector. In addition to demonstrating the elimination of the dead zone, a new loop filter is described. The filter takes advantage of the new phase detector circuit technique so as to simultaneously provide both low-level reference sidebands and a lock-up time of one cycle of the reference.

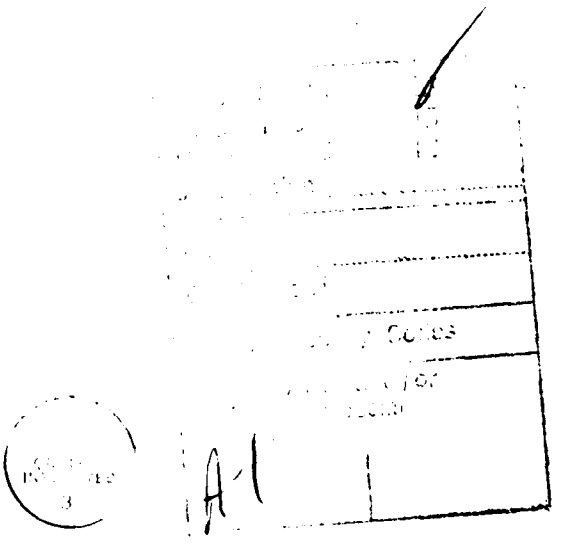


TABLE OF CONTENTS

LIST OF FIGURES

I. INTRODUCTION

Phase detectors are used in control systems to measure the phase of one signal relative to the phase of another signal. Control systems of this type are usually referred to as Phase-Locked-Loops (PLL). Figure 1.1 shows a basic Phase-Locked-Loop. The loop is shown with a divide by N frequency divider connected in the feedback loop. For the phase of the output of the frequency divider to track that of the incoming signal, the controlled frequency source must be producing a frequency of exactly N times the frequency of the incoming signal. This property is used in various applications.

Development of phase detectors has occurred because of the PLL application. A new phase detector is described in this paper. This circuit is the result of research into improving the characteristics of the PLL; specifically, PLL's with digital control loops (such as the divide by N circuit). The new phase detector operates with binary signals as inputs and is used as an element in high-performance frequency synthesizers.

Problems with PLL oscillators include that their output spectrum is not pure, and that they suffer from cycle to cycle random time jitter. The new circuit was designed during the construction of an fast tuning, ultra low noise

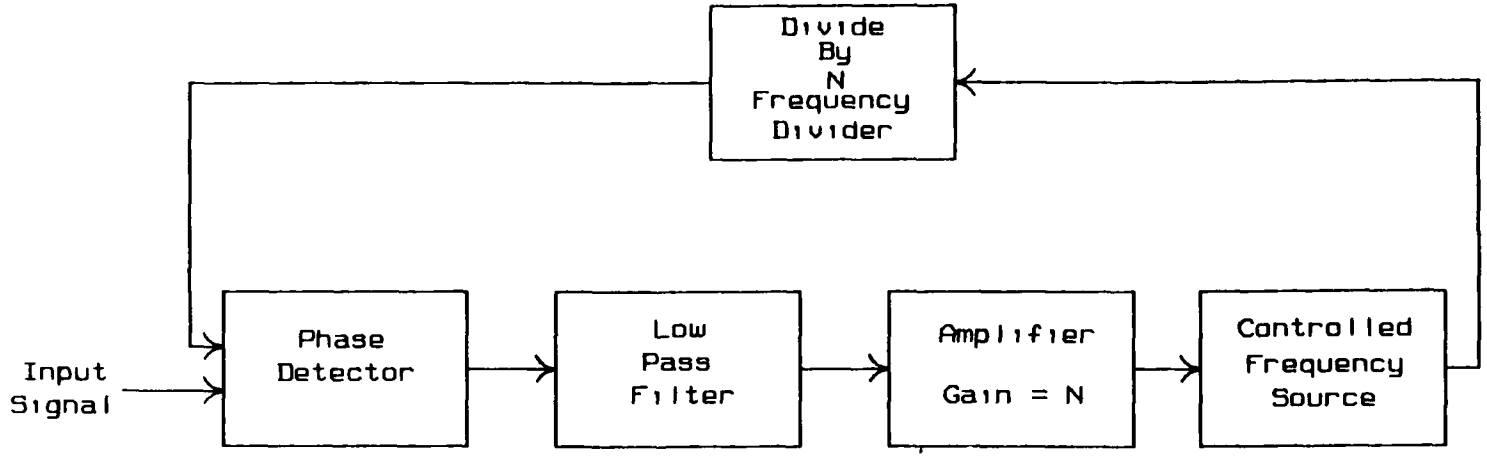


Figure 1.1 Basic Phase Locked Loop
Shown With A Frequency Divider In The Feedback Loop.

phase-locked coherent oscillator for use in a pulse doppler radar. In this application, precise transition times were extremely important. In order to obtain the lock-up speed required, while simultaneously achieving low noise, a circuit using a standard digital type of phase/frequency detector was constructed. It fell short of the performance expected due to a dead-zone in the phase detectors transfer function. The new circuit eliminates the dead-zone and allows a superior loop filter to be built. The resulting circuit was constructed, tested, and shown to work. Chapter VI. contains photographs of oscilloscope traces verifying its operation.

It is important to realize that a phase detector is different from a phase-locked-loop. A PLL is a system made up of several parts. A phase detector is just one of the parts used in a PLL system. This thesis will describe a new phase detector circuit. A PLL is only one application where the new phase detector may be useful.

II. BACKGROUND

In much of the literature on phase-locked-loops, the controlled frequency source (CFS) is implemented with a voltage controlled oscillator (VCO). Conceptually the VCO definition is appealing since it implies very fast tuning characteristics. However, this speed is not always available. For example, motor driven microwave cavity oscillators have been used in phase-locked-loops as the controlled frequency source. In motor speed control applications, the motor itself is the controlled frequency source. In this report, VCO refers to the frequency source being controlled even though many applications do not use a VCO.

Frequency synthesizers and coherent oscillators are usually required to be single-frequency sources. Other energy in the output of these oscillators (energy at other than the desired frequency) is undesirable. Two types of other energy do appear however: broadband noise, and "spurs". A spur refers to a clearly defined frequency that appears in the spectrum of the oscillator output, but it is not at the desired frequency.

A particular problem with PLL oscillators is that "reference frequency spurs" are above and below the primary output frequency. The term "reference frequency spurs" is

given because the spurs are caused by modulation of the VCO at the reference frequency. The modulation causes spurs to be generated a frequencies separated from the primary frequency by the frequency of the reference signal. This problem occurs because the phase measurement is done on a cycle by cycle basis of the reference frequency, and therefore the tuning voltage that controls the oscillator also varies cyclically with the reference frequency. The oscillator is thus frequency modulated to some degree, and spurs are generated.

Another problem in phase locked loop (PLL) oscillators, is that the dynamic tracking accuracy of the voltage controlled oscillator (VCO) is a function of the loop gain and bandwidth. To minimize the effect of VCO noise on the output signal purity, the loop gain and bandwidth need to have large values. To minimize the reference frequency spurs, however, the loop response must attenuate the reference frequency and its harmonics, which calls for small values of loop gain and bandwidth. Clearly a problem exists in meeting both criteria simultaneously. For example, a sharp cutoff multi-pole filter could be used to attenuate the reference frequency and its harmonics. This attenuation would allow the gain to be higher without excessive reference frequency feed through. However, the delay through a filter is related to the sharpness of the filter cutoff. Due to the increased time delay, the loop gain must be

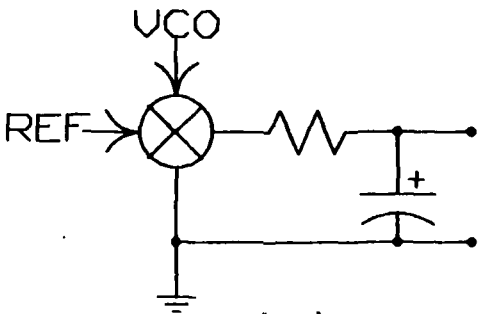
reduced to maintain stability. But that gain reduction contradicts the purpose of the multi-pole filter, which was to allow the gain to be high. The outcome is that some other technique must be used if the VCO spectral purity is to be improved. The problem can be further identified by inspecting the response of a common mixer type of phase detector to various input signals.

A. THE STANDARD MIXER TYPE OF PHASE DETECTOR

Figure 2.1 shows two common "mixer" types of phase detectors. Mathematically a mixer type of phase detector is a multiplier followed by a low pass filter. If two sine waves are in phase and multiplied together, the output is a sine wave of twice the frequency plus a DC term. That is, $\{A \sin(wt)\}\{B \sin(wt+\theta)\} = AB/2 \cos(\theta) - AB/2 \cos(2wt+\theta)$. The low pass filter removes the high frequency ($\cos(2wt)$) term but passes the DC ($\cos(\theta)$) term. Clearly, the DC term is a function of the phase between the two input signals. If the two signals are 90 degrees out of phase, then there is no DC term. If the two signals are 180 degrees out of phase, then the DC term is negative. In practice, the low pass filter usually does not eliminate the high frequency term, but only attenuates it.

We will now show that a common mixer has four major problems when it is used as a phase detector in a PLL.

1. The error slope of the mixer reverses every 180 degrees. This causes the sign of the feedback to reverse in a PLL.



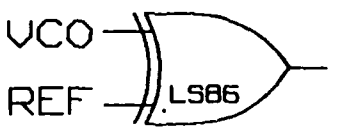


Figure 2.1 Mixer Type Phase Detectors.

2. A signal at twice the reference frequency appears at the output.

3. The output of a mixer does not indicate whether the VCO frequency is above or below the reference frequency.

4. An error slope is obtained when the inputs are odd harmonics of one another. This fact can cause a PLL to lock onto an undesired frequency.

These problem can be seen most clearly graphically.

Figure 2.2 graphically shows the operation of a mixer type of detector when square waves are used as the inputs. Phase will be defined by the distance between low-to-high edges of the two signals. In the case of Figure 2.2 diagram (a), the VCO is at -90 degrees. That is, the low-to-high edge of the VCO is to the right of the low-to-high edge of the reference signal by 90 degrees. Diagrams (a), (b), and (c) show the normal mixer operation. Diagram (a) shows the case where the VCO is lagging (to the right) the reference signal by 90 degrees. Note that the output averages zero (there is no DC term). If the detector output were the error signal in a phase locked loop, this would be the ideal lock point (no error). Figure 2.2 (b) shows the case where the VCO leads the -90 degree zero output voltage point. Note that the output averages a negative voltage. Figure 2.2 (c) shows the case where the VCO lags the -90 degree zero output voltage point. Note that the output averages a positive voltage. From these three diagrams we see that the output polarity could be used to drive a VCO toward the zero-output point.

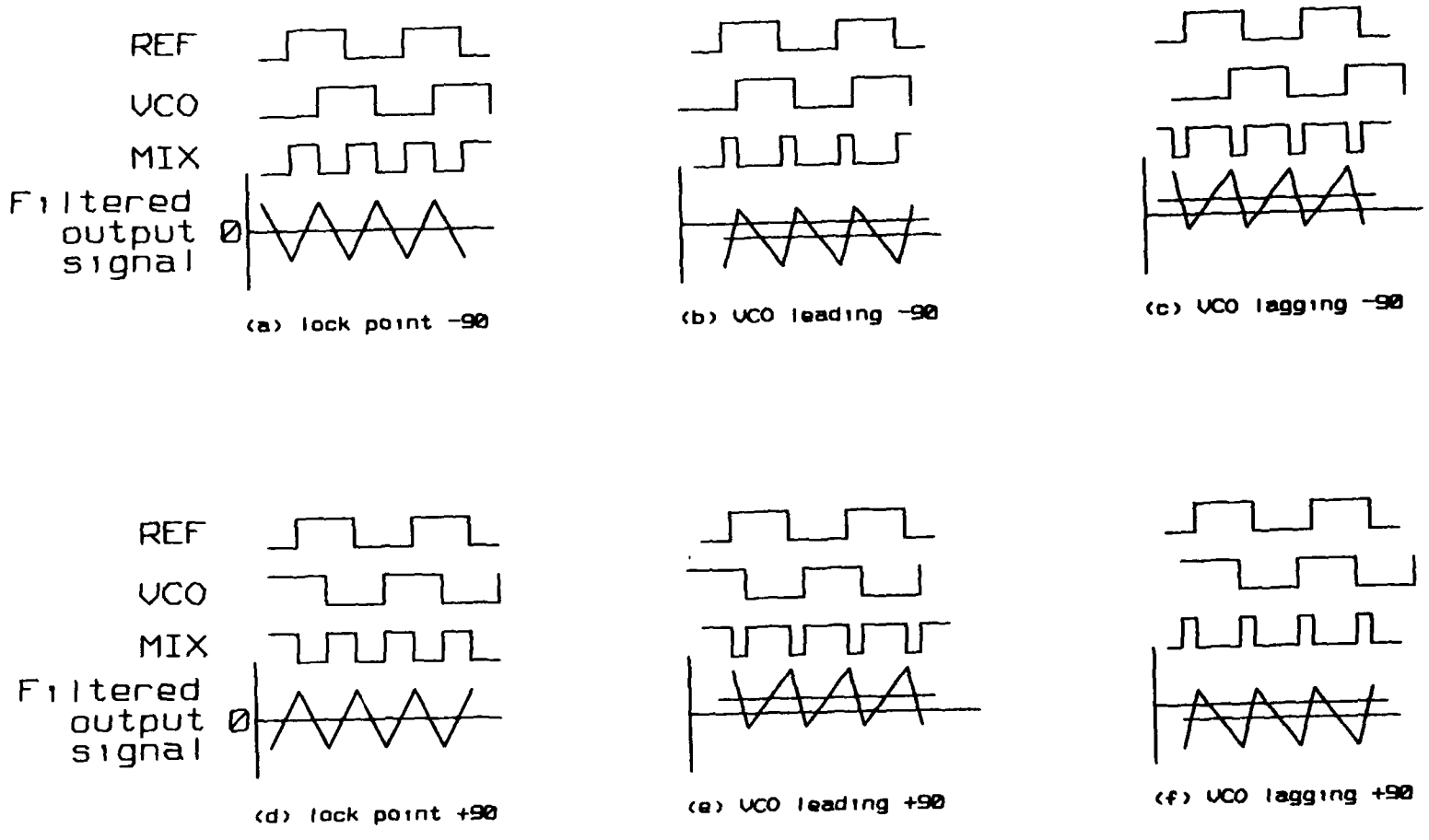


Figure 2.2 Response of a Mixer Type Phase Detector With Bipolar Square Wave Inputs.

Suppose the frequency of the VCO were locked as shown in (a). If the VCO frequency drifted lower, then we would expect the mixer output to go higher as in (b). If the VCO frequency drifted lower, then we would expect the mixer output to go higher as in (c). Suppose a VCO was made with a tuning function such that a higher voltage produced a higher frequency, and the correct frequency was produced at near zero volts (as for example, the tuning curve shown in Figure 2.3). Its operation with a mixer phase detector operating as in Figure 2.2 (a), (b), and (c) would result in a stable negative feedback loop. With this background, it is now easy to show how problem #1 occurs.

Problem #1 is highlighted by Figure 2.2 (d), (e), and (f). Diagrams (d), (e), and (f) are identical to (a), (b), and (c) except for a 180 degree phase shift. The result is that the error in (b) is opposite the error in (e). And the output in (c) is opposite the output in (f). Recall that the mixer output was a function of cos(ß). If the resting point is ß=+90 degrees then the slope of the output voltage to phase shift has one sign. But if the resting point is ß=-90 degrees, the the slope of the output voltage to phase shift has the other sign. If the VCO from above were connected to a mixer phase detector operating as in (d) (e) and (f), then the feedback would have the wrong polarity. This is, in fact, what happens in practice. So if a mixer is used as the phase detector within a phase locked loop, then

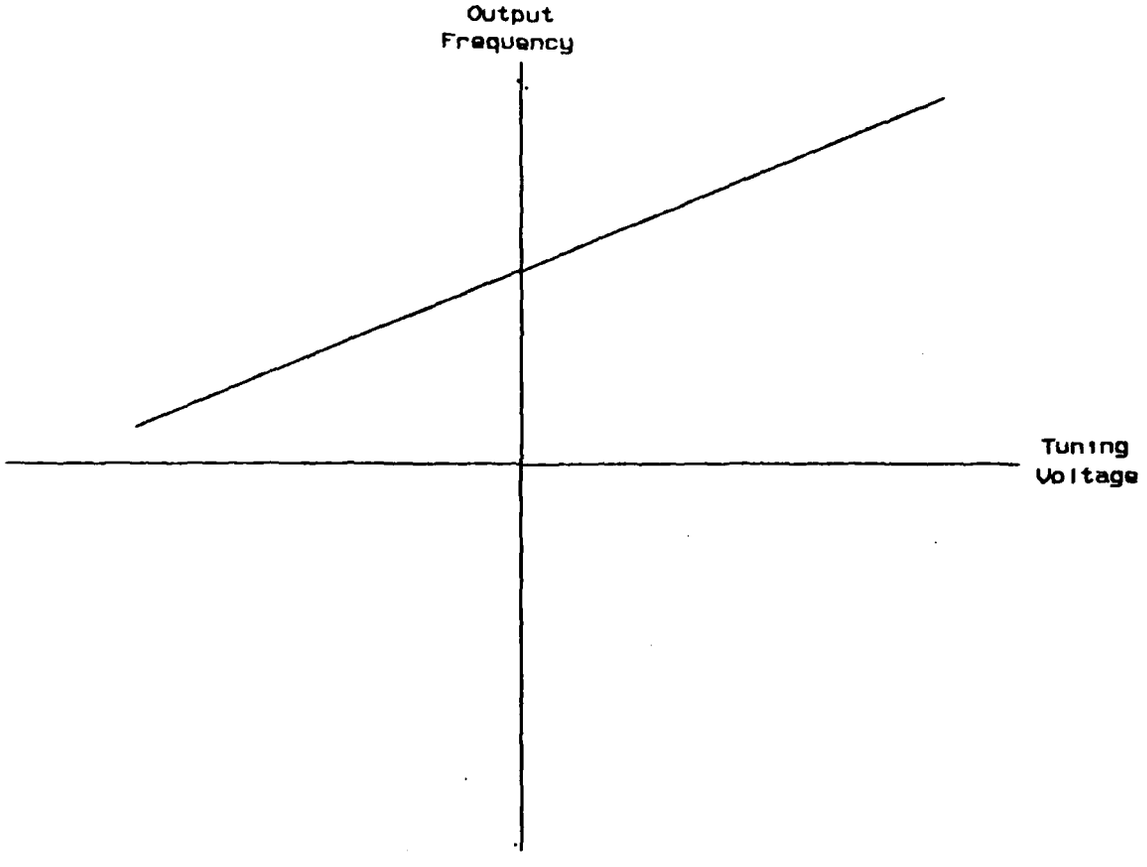


Figure 2.3 Typical VCO Tuning Curve.

it will sometimes drive the VCO away from the desired frequency. This problem causes instability and poor lock-up performance in PLLs.

Problem #2 can be seen clearly in all of the mixer response diagrams. There is a large component at twice the reference frequency, in the output signal. Notice that even with the large phase shifts used to illustrate the phase detection, the double-frequency component is much larger. Adequate filtering of this large signal is sometimes impossible (as was discussed prior to looking at the mixer diagrams).

Problem #3 is illustrated by Figure 2.4. It shows the output from a mixer type of detector with two input signals of slightly different frequencies. The output oscillates at the difference frequency between the two input signals. Because the output is not a single polarity, one cannot tell from looking at the output signal whether the VCO frequency is above or below the reference frequency. As a result, a VCO in a PLL will not always be driven toward the lock point. This problem causes a PLL to not acquire lock unless the VCO frequency is close to the reference frequency. And it causes the loop to lose lock easily in the event of transients.

Problem #4 is illustrated by Figure 2.5. It shows the output of a mixer type of phase detector when the VCO and reference frequencies are odd harmonics of one another. The

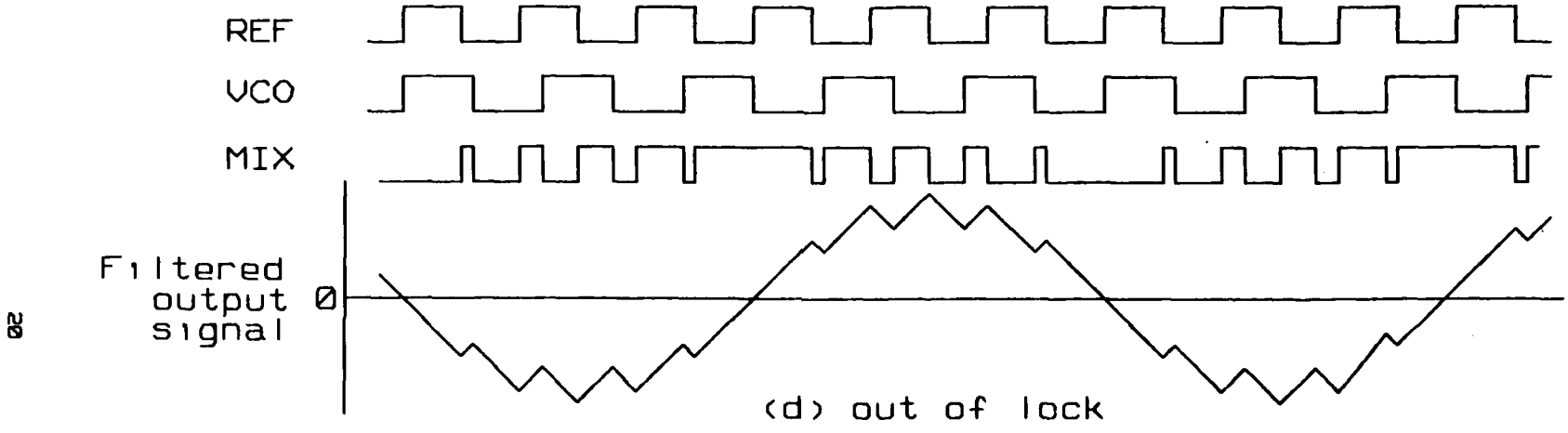


Figure 2.4 Response Of A Mixer Type Phase Detector With Unmatched Frequency Inputs.

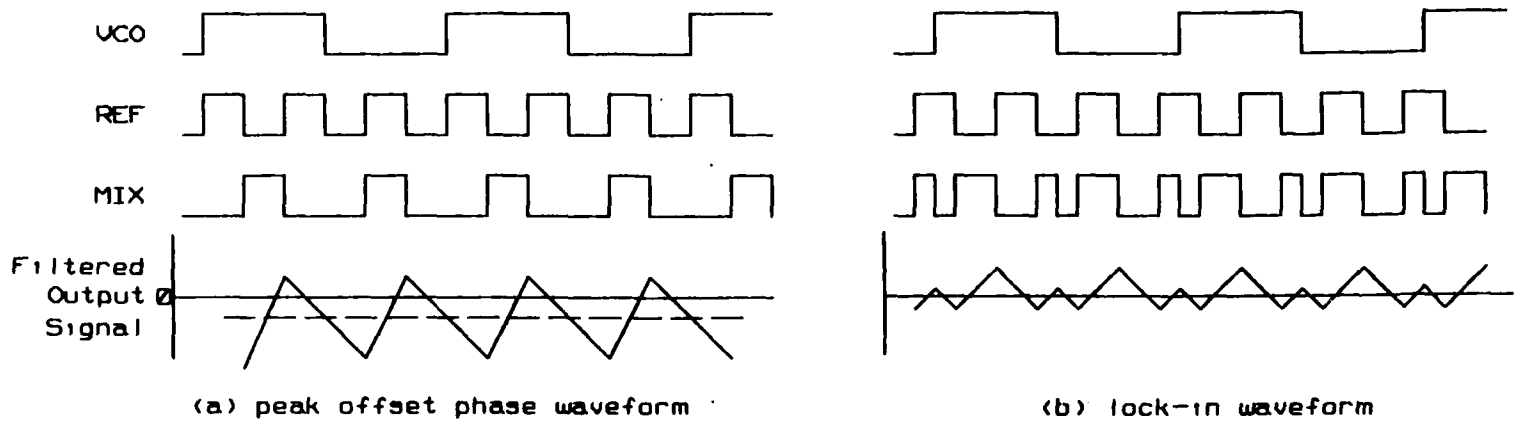


Figure 2.5 Response Of A Mixer Type Phase Detector
With Odd Harmonics.

mixer produces an output identical to the matched frequency case except that the DC offset term is smaller. The result is that PLL's using a mixer as a phase detector may lock onto odd harmonics of the reference signal.

B. THE DIGITAL PHASE DETECTOR

One technique used to combat both the conflicting loop gain and bandwidth requirements, and the complications arising from the mixer type of phase detector, is the digital phase/frequency detector. The digital phase/frequency detector has been described in the literature and has been made into monolithic integrated circuits such as the Motorola MC4044 TTL version and the RCA CD4046 CMOS version. Descriptions of these circuits can be found in the manufacturers data books. The digital phase detector eliminates all four of the problems listed for the mixer type of detector.

The name "phase/frequency detector" is somewhat troublesome. It is common in literature not to differentiate between a demodulator and a detector. As a result, the terms are not well defined. One definition for a detector is that a detector is only required to indicate the presence of a signal; a binary yes/no. In the case of frequency, it might detect whether the frequency of one signal is above or below that of another signal. It is this definition that is being referred to for the "frequency" part of the name "phase/frequency detector." The "phase" part of the name

refers to another definition. That definition states that a detector produces a signal which varies in some manner, as a function of its inputs. In the digital phase/frequency detector for example, the output is a pulse width modulated signal, where the pulse width is proportional to the phase difference between the two signals. (Unless, of course, the two signals are not the same frequency, then the other definition is used and the output is high or low depending on which signal frequency is above or below the other). It is hoped that this discussion will prevent concern over the name given in the Integrated Circuits Databooks, and hence the name used in this report that refers to the device as a digital phase/frequency detector.

1. The Digital Phase/Frequency Detector Operation

The CD4046 is used to illustrate the detector operation. The CD4046 has two comparators. This discussion will focus on comparator II since it is the type of phase detector of interest. It has two inputs, one for the reference frequency (REF), and one for the feedback frequency (VCO). These inputs are only sensitive to low-to-high transitions. The output of the phase detector has three states, high (pulled to the positive supply line), low (pulled to the negative supply line), and open circuit. A secondary output (called LOCK) is either high or low. The LOCK output is high whenever the output is in the open

condition; otherwise it is low. The rules governing the output are as follows.

If the two inputs signals are at the same frequency, then:

1. If the VCO input leads REF input by ß seconds, then the output is pulled high at the leading edge of VCO input and goes back into the open circuit state at the leading edge of REF input. It therefore remains high for ß seconds and then goes into the open state.

2. If the REF input leads VCO input by ß seconds, then the output is pulled low at the leading edge of REF input and goes back into the open circuit state at the leading edge of VCO input. It therefore remains low for ß seconds and then goes into the open state.

3. If the leading edge of both inputs occurs simultaneously, then output (C) remains in the open circuit condition.

If the two inputs are not the same frequency then:

4. If the VCO input signal frequency is above the signal frequency on the REF input, then the output is pulled high.

5. If the VCO input signal frequency is below the signal frequency on the REF input, then the output is pulled low.

Operation of the digital phase/frequency detector can be shown graphically. Figure 2.6 (a) shows a simple PLL with the CD4046 digital phase/frequency detector connected to a simple RC filter. The diagram in (b) shows the output of the phase detector with the VCO leading, then equal, and then lagging the reference signal. Because the output is open circuited, the charge on the capacitor is either increased or decreased with the output pulses from the phase detector, but otherwise retains its charge and

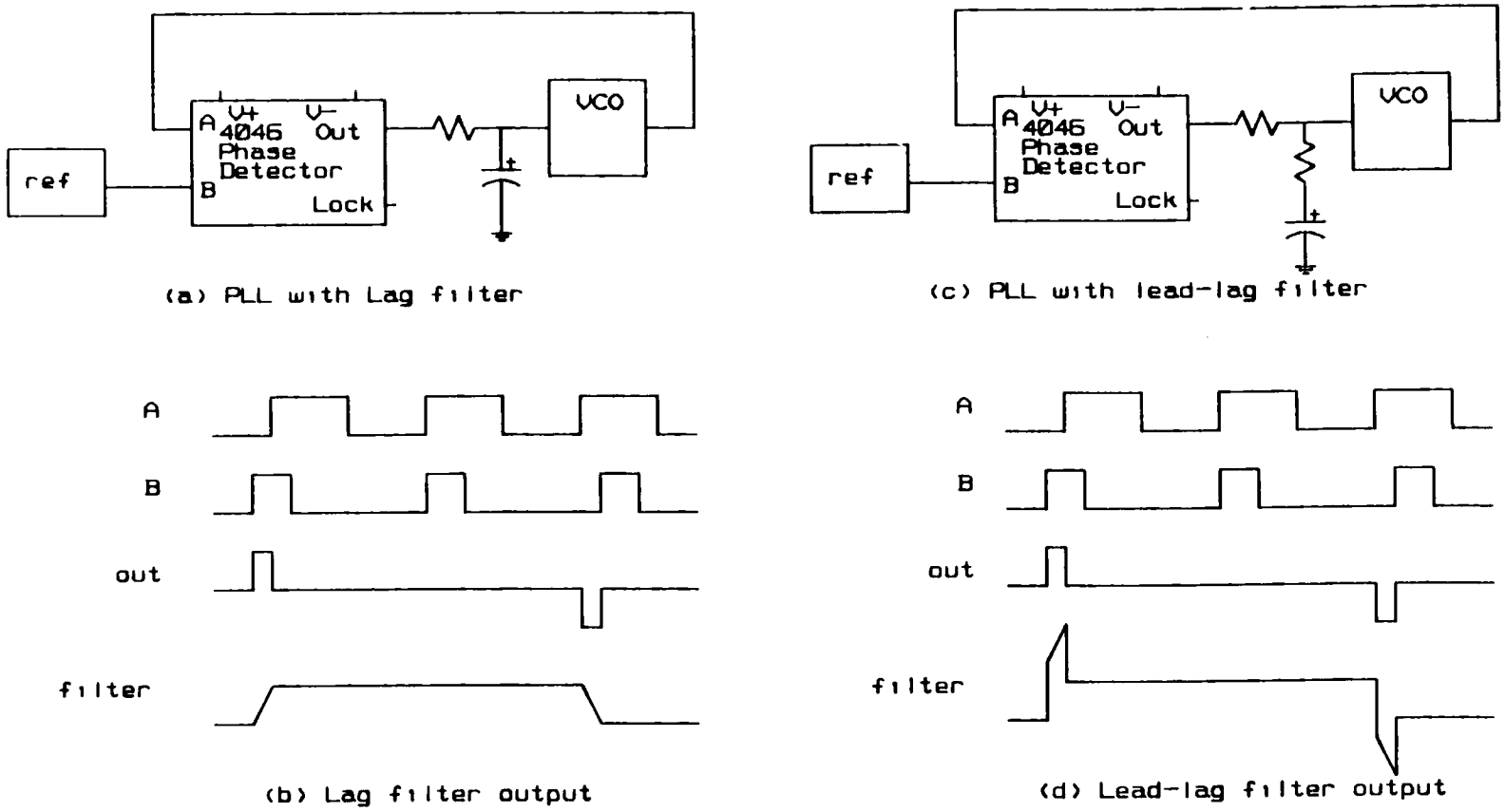


Figure 2.6 Response Of A Digital Phase/Frequency Detector.

voltage. The manufacturers data books refer to the output as a charge pump. That is, the charge on the capacitor is pumped up or pumped down by the output pulses.

Clearly, from rules 4 and 5, the digital phase detector will always steer the VCO toward the lock point. Figure 2.6 (b) clearly shows that very little filtering is required to remove any ripple component. In fact, ideally there is no steady state ripple. Once the VCO is at the proper voltage, the phase detector output just remains open circuited.

Another benefit from this type of phase detector is the ease with which an optimal time control loop can be constructed. When the settling time must be minimized for a shift in operating frequency, a lead-lag network can be chosen such that the loop settles in one cycle. A common application of this technique is in frequency synthesizer design where it is desired that a change in "N" (for the divide-by-N counter between the VCO output and the phase detector) be accompanied by a very quick change in the VCO frequency.

To accomplish this one cycle settling, the phase of the VCO must be "bumped" and the steady state voltage must be shifted to a new value corresponding to the new operating frequency. The "bump" in phase is necessary because phase-shift between the reference and VCO accumulates over the period of one cycle before it is measured. As a result,

the diodes block any current from charging C1. A string of

if all the error voltage were applied to changing the frequency of the VCO, the frequency would be shifted too far. The "bump" in phase is really a temporary excess shift in frequency to allow the phase of the VCO to catch up to the reference phase. Figure 2.6 (c) shows a loop using a lead-lag filter. The diagram in (d) shows the "phase bump" coming out of the filter. Note that the "bump" width is variable and occurs while the phase detector is not in the open circuit state.

2. The Lock-in Point Dead Zone Problem

There is, however, a problem with the digital detector at the lock-in point. There is a non-linearity, a dead zone, in the output voltage at the zero phase point. In a closed loop system, this non-linearity causes the phase of the VCO to drift randomly +/- δ degrees from the zero phase point. The drifting causes spreading of the spectrum in the frequency domain and can cause time sensitive systems to malfunction due to random variation. The non-linearity is caused by the finite switching speed of the devices used in the digital detector. The magnitude of δ is a function of the circuit path time-matching and is a function of the switching speed of the devices used to implement the digital phase detector.

The problem occurs because very small time differences between the two input signals allow insufficient time for semiconductor devices in the output stage to change

C. VOLTAGE TO CURRENT CONVERSION AND OFFSET INSERTION

The voltage on C1 is measured by a very high input

states. The output is supposed to go from an open circuit state, to a high or low state, and then back to an open state. Instead, the output just remains in the open circuit state. The net affect is a dead zone centered at the zero phase point. The width of the dead zone is a function of the speed of the devices used. The faster the devices, the narrower the dead zone, but there will always be a dead zone.

3. The Spike Problem

A secondary problem with the digital phase detector is the narrow spike that is generated when a lead-lag filter is used. It can be seen in the last trace of Figure 2.6 (d).

The spike causes extremely high peak control signals to be generated (which is a problem for motor control systems). The spike also causes spectral spurs to be generated at many harmonics of the reference frequency (which is a problem for synthesizers). Whenever fast settling time is required, this spike becomes a serious problem.

The circuit designer's dilemma is that the "bump" in phase is caused by a voltage spike that is very narrow with respect to the period of the reference waveform. Because of the large difference between the reference period and the spike period, filtering of the spike while retaining the one-cycle settling is not practical.

III. THEORY OF OPERATION OF THE NEW CIRCUITS

A. PHASE/FREQUENCY DETECTOR

The circuit presented here provides a phase detector with all the advantages of the digital phase detector but eliminates the dead zone inherent in the original design. The technique used to eliminate the dead zone also allows the filter to be optimized such that one-cycle settling can be obtained without the narrow spike like "bumping" pulse but instead, with a broadly shaped pulse.

A detailed description of the circuit is contained in chapter V. The theory behind the new phase detector, is to shift the lock point (the steady state operating point), off the zero-phase point where the dead zone lies. The lock point is shifted by requiring the digital phase detector to produce an output on a cycle by cycle basis that cancels an external offset. To prevent the external offset from influencing the VCO, the digital detector output-plus-offset is sampled after each cycle. The sampled error signal becomes the output for the new phase detector. The important facts to understand at this point are:

1. The phase detector output is a bipolar current.
2. The amplitude of the output current is proportional to the phase difference between the two input signals (plus an adjustable offset).
3. The output current is only enabled for a fraction of the reference period.

4. The time duration that the output current is enabled can be adjusted independently of the reference frequency.

Figure 3.1 is a simplified block diagram of both the new phase/frequency detector and the new loop filter. At the end of an output pulse from the 4046, the LOCK output triggers one-shot A. One-shot A generates a pulse that closes the output switch enabling current to flow through the output. The end of this pulse triggers one-shot B. One-shot B generates a pulse that closes the switch shorting out capacitor C1. In order for the output current to be zero, C1 must be charged just enough to counteract the offset added to its voltage. The voltage offset therefore forces a fixed phase shift at the lock-in point.

In the event that the two input frequencies are different, the LOCK output will remain low. In that case, to insure that the output switch is closed, the off-frequency-logic circuitry will trigger the output switch since the LOCK line will not.

B. LOOP FILTER

Since the time duration of the output current is independent of the reference frequency and phase, the output duration and loop filter can be chosen to simultaneously provide both optimal one-cycle settling time and low reference sidebands. The "pump-up" and "pump-down" gains are forced to be equal and independent of the VCO tuning voltage by virtue of the current source output. By making

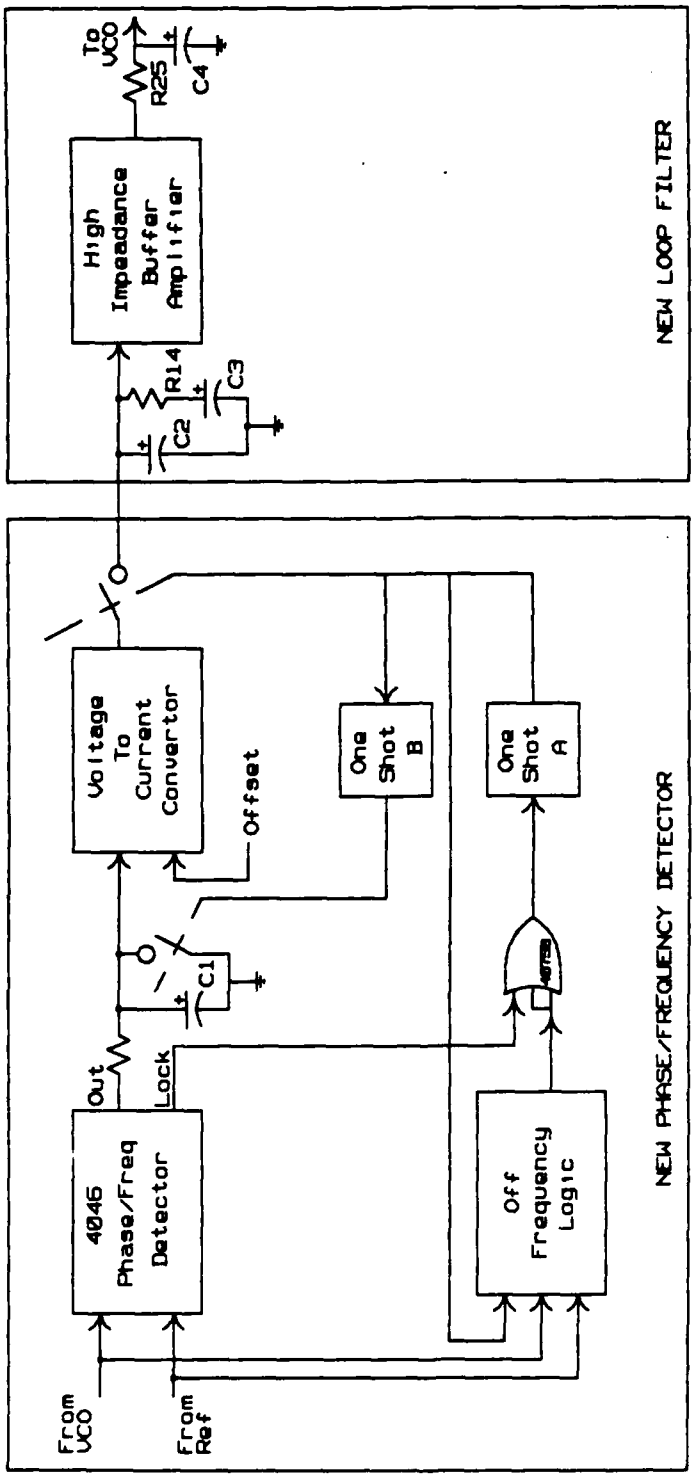


Figure 3.1 Block Diagram of the New Phase/Frequency Detector and New Loop Filter

the output duration a significant time period with respect to the reference period, the "spike" (referring to the standard phase/frequency detector) is converted to a broad hump.

The new loop filter shown in Figure 3.1 was designed to produce a broad hump while simultaneously providing one-cycle settling of the loop to a frequency change. The component numbering matches Figure 5.1, the schematic of the new phase/frequency detector circuit. A pulse of current going into the network will charge C2 faster that C3 due to the resistance of R14. At the end of the pulse of current, the voltage on C2 will come down in order to charge C3, until equilibrium is reached where C3 and C2 have the same voltage. The network, therefore, produces a broad "bump," with the final voltage slightly different from the initial voltage. The ratio between C2 and C3 determine the height of the "bump" over the final value. R14 determines the settling time of the voltage on C2. R25 and C4 smooth the resulting pulse and affect the settling time of the overall pulse.

In order to gain further insight into the filter operation with the new detector, chapter IV shows the results of a computer simulation of the filter network, and a complete phase locked loop using the new detector and new filter.

IV. COMPUTER SIMULATION

It was not the intent of this thesis research to analyze or optimize or demonstrate the acquisition speed of a PLL using the new phase detector and filter. However, acquisition and use of "TUTSIM", an IBM-PC program that does continuous dynamic system simulation, allowed simulation of both the loop filter dynamics, and the closed loop dynamics. Appendix A contains a brief description of some of the TUTSIM model blocks. It includes listings of the simulation models which may be useful to experienced users of TUTSIM. Block diagrams of the models are also shown in Appendix A. Discussion of the models is beyond the scope of this report. The simulation results are included here only to provide greater insight into the operation of the new phase detector and filter as it applies to phase-locked-loops.

A. SIMULATION OF THE NEW LOOP FILTER

Figure 4.1 shows the results of a computer simulation of the new filter. It is being driven with a fixed current input (corresponding to a fixed phase error from the new detector). The plot starts at t=0- in a steady state condition. At t=0+ the phase detector output is enabled and the filter pulse is started. The square pulse is the current dumping into the filter network. The ramp is the output of the C2, R14, C3 network. The curved ramp is the

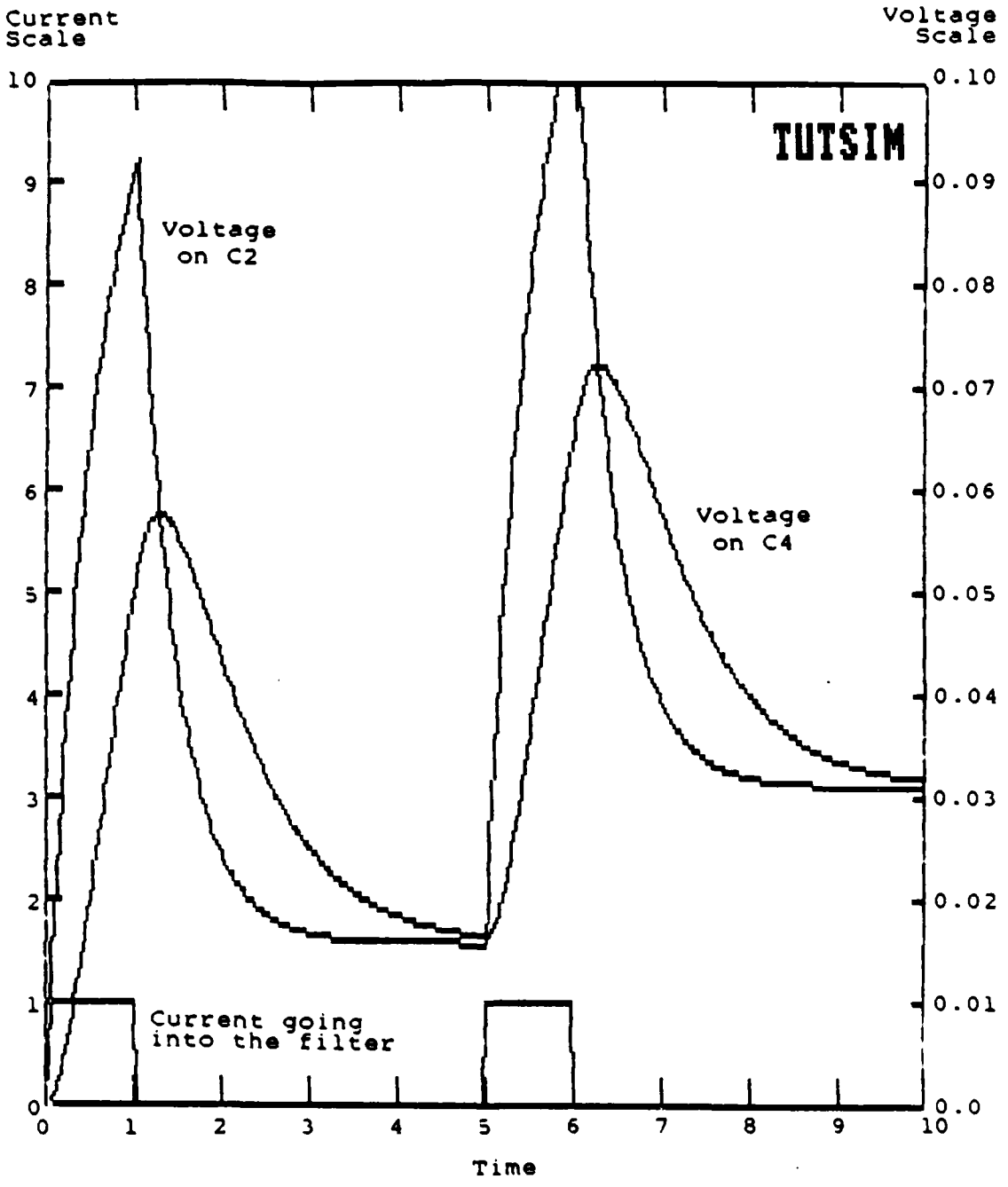


Figure 4.1 Loop Filter Time Domain Performance

output of the R25, C4 part of the filter. At t=0.2 the phase detector output current is disabled and the filter output begins to ramp down. At t=1- the filter output is almost settled. And at t=1+ the next output from the phase detector occurs. One can see clearly how the narrow "spike" shown in the last waveform on Figure 2.6 (d), has been replace by a very small broad "bump" in Figure 4.1 since the area under the two "bumps" must be equal.

B. SIMULATION OF A PLL USING THE NEW PHASE/FREQUENCY DETECTOR

Figure 4.2 shows what happens for both a step change in frequency and a step change in phase. The loop is steady state up to t=0-, at t=0+ a frequency change is introduced. At t=1 the phase detector output is enabled and the filter pulse is started. The square pulse is the current dumping into the filter network. The ramp is the output of the C2, R14, C3, R25, C4 filter network. At t=0.2 the phase detector output current is disabled and the filter output begins to ramp down. The scale was set purposely to let the filter output go off the scale so that a close look at the one-cycle lock could be observed. At t=2- the loop is almost settled. At t=2+ a very small current pulse occurs indicating almost perfect one-cycle settling. The circuit values were chosen interactively so perfect settling was not expected.

At t=3.5 a phase offset was put into the simulation. At t=4 the sampler sees the error and begins to correct it.

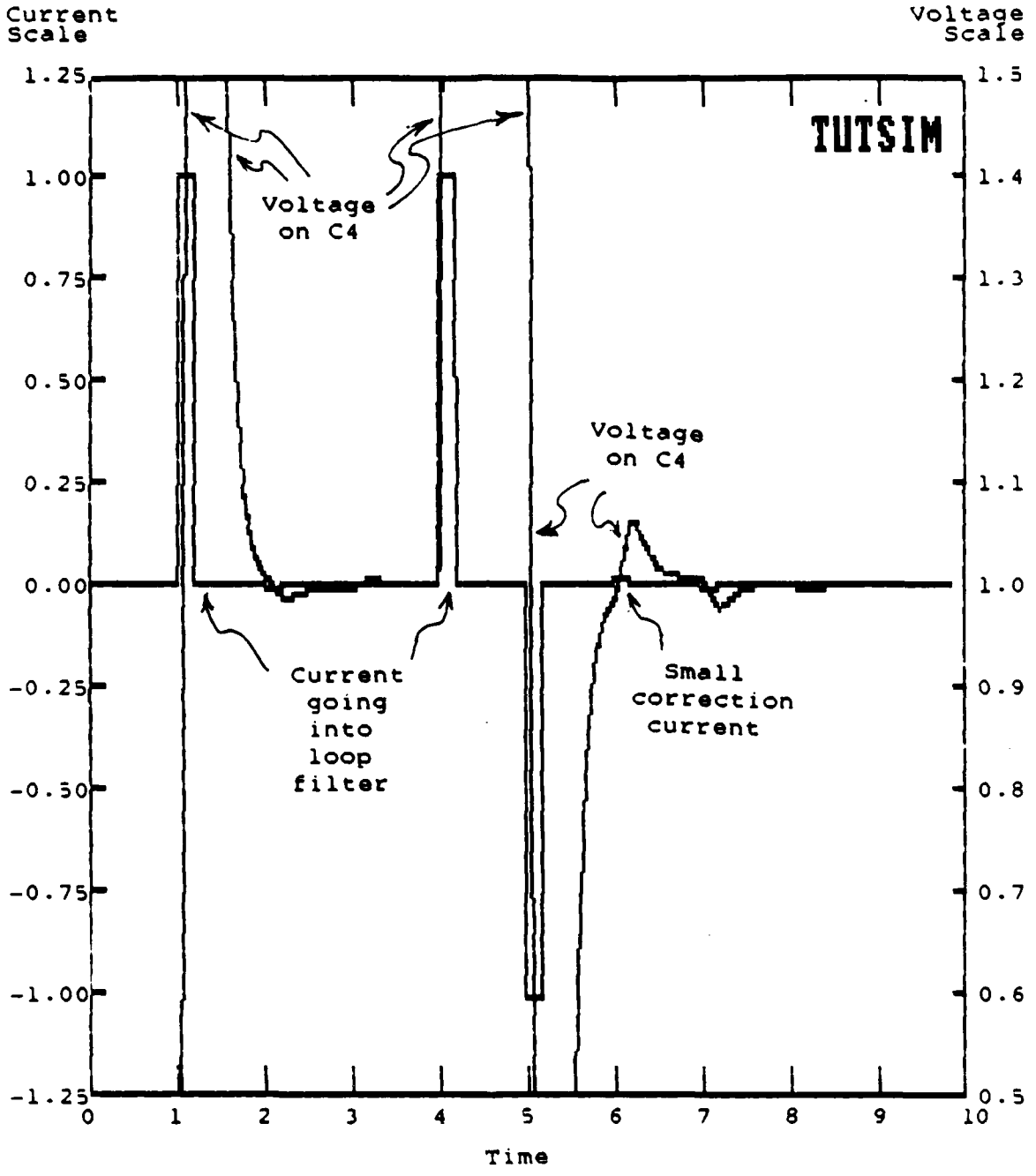


Figure 4.2 PLL Time Domain Performance

Note that since the filter was designed to optimally correct frequency errors; the phase error was interpreted as a frequency error. To correct the phase shift, the frequency must be temporarily changed. At t=5 the frequency error is detected and a pulse of the opposite polarity brings the loop back into lock. At t=6 the loop is essentially settled again. Thus, the response to a phase shift step takes two cycles of the reference frequency to re-lock.

V. DETAILED CIRCUIT DESCRIPTION

The circuit description will follow the schematic diagram shown in Figure 5.1.

A. INPUT STAGE

The two input signals, the reference frequency signal and the VFO signal are first level shifted and amplified. Input capacitors C7 and C8 act as DC blocking capacitors. Potentiometers R23 and R24 establish the DC bias point for U1 a CD4011B CMOS NAND gate. The potentiometers are adjusted according to the duty cycle of the input signals. The NAND gate amplifies and squares the input signals.

B. STANDARD DIGITAL PHASE/FREQUENCY DETECTOR AND OUTPUT STORAGE

The output of the input buffer U1 is fed to a CD4046 which contains the standard digital phase detector. The output is fed through a set of transistors connected to function as diodes. The purpose of these diodes is to allow leakage current from the CD4046 to be isolated from the storage capacitor C1. The desired function for the diodes would be that of a very low voltage, perfect zener diode. Transistors are used since they create a diode with a much sharper turn-on characteristic than standard diodes. As long as the leakage current flowing into R0 produces less than 0.4 volts, and the voltage on C1 has been reset to 0 volts,

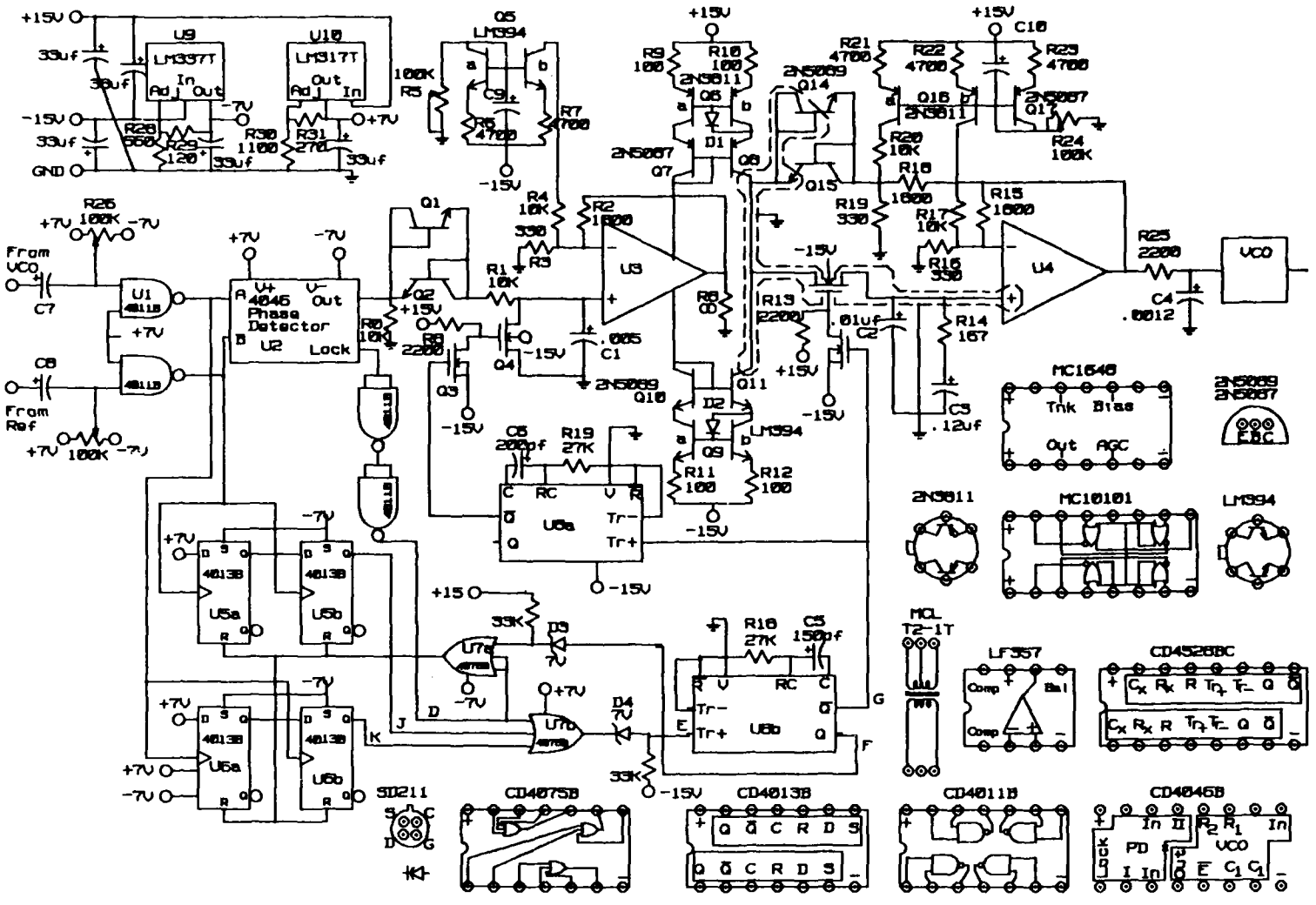


Figure 5.1 Schematic of the New Phase/Frequency Detector and Filter.

the diodes block any current from charging C1. A string of transistors or a zener diode could be used if a higher isolation voltage were desired. This is unnecessary for this circuit since one is primarily concerned with this leakage in the steady state condition. And in the steady state condition C1 will be charged only slightly.

The output pulse from the U2 lasts for the duration of the phase offset between the two input signals. R1 and C1 integrate each pulse coming from U2. As such, they establish the gain (Volts/Degree) of the offset insertion section. C1 only accumulates charge based on one output pulse from U2. Transistor Q4 shorts C1 to reset it after the value on C1 has been passed to the output via Q12. Thus C1 is now ready to integrate the next pulse coming from U2.

The gain can be calculated as follows:

1. Using a reference frequency of 60 kHz, the time corresponding to 1 degree of phase shift is:

   1/360 degrees * 1/60 kHz = 46.3 ns.

2. Since C1 will always be close to ground potential, the current flowing into C1 will be:

   (Voltage at the input side of the R1)/R1 = 6 Volts/ 10 K ohms = 600 ua.

3. And the voltage on the C1 will be:

$$\frac{600\ ua * 46.3\ ns}{.005\ uf} = 5.6\ mv. \quad or \quad 5.6mv/degree$$

If it is assumed that the lock-in point is offset by 10 degrees, then the voltage on C1 will be .056 volts after being charged.

C. VOLTAGE TO CURRENT CONVERSION AND OFFSET INSERTION

The voltage on C1 is measured by a very high input impedance amplifier (U2) to prevent its charge from being disturbed. U2 is an LM357 FET input op-amp. The amplifier is set up in a non-inverting mode to maximize the input impedance.

A current mirror is a device with a low impedance input port and an extremely high impedance output port. Whatever current is pushed into (pulled out of) the input port, is reflected and pulled out of (pushed into) the output port. Due to the high output impedance, the output current is independent of the output voltage.

Transistors Q6, Q7, and Q8 form a high precision current mirror. Transistor Q7 is included to force the collector voltages on Q6a and Q6b to be matched. This matching causes more precise current mirroring to occur. Diode D1 is included to increase the collector voltages on Q6. The effect of the higher voltage is to reduce the collector capacitance.

Transistors Q9, Q10, and Q11 and D2 form another current mirror but with the opposite polarity of the Q6 based mirror.

The power supply terminals of U2 are connected to the current mirrors to provide a voltage to current conversion function. The voltage at the output of U1 is converted to a current. The amplitude of the output current is equal to

whatever current flows out of the amplifier output. This conversion is based on the fact that if no current is flowing out of the amplifier output terminal, then the current flowing into the + power supply terminal must be exactly balance by the current flowing out of the - terminal. Since these two currents must be exactly the same, the currents coming out of the Q8 based current mirror and the currents going into the Q11 based current mirror must also be the same and therefore cancel. An output current can only appear when current flows out of a different path from the amplifier. Since the FET inputs to the amplifier draw negligible current, this only leaves the output port.

While output resistor R8 is shown on the schematic, the feedback resistors R2 and R3 were selected to provide the necessary output loading on U2. Therefore R8 is shown with a value of infinity.

The voltage to current conversion factor can be calculated as follows:

1. The non-inverting gain is:

   1 + R2/R3 = 1 + 1800/330 = 6.45 Volts/volt

2. The equivalent resistance that the op-amp drives is:

   R2 + R3 = 1800 + 330 = 2130 ohms

3. The conversion factor is:

   6.45/2130 = 3.03 ma./volt

Previously the voltage on C1 was calculated to be 5.6 mv/degree. Now we can convert that to a current as follows:

5.6 mv/degree * 3.03 ma./volt = 16 ua./degree

The offset is inserted by an adjustable current source. This function is provided by Q5a and Q5b. Q5 is a matched pair of transistors. The pair of transistors are connected in a very simple current mirror configuration. The current mirror makes the offset current equal to the current going through potentiometer R5.

The phase of the steady state lock-in point is thus adjusted by R5. If the lock-in point is close to zero phase difference, then R5 will be a large resistance and little current will be inserted. In this case only a small voltage would be required on C1 to cause the amplifier output current to be equal and opposite to the offset current. And the small C1 voltage translates to a small phase difference between the two input signals.

D. LOOP FILTER AND OUTPUT BUFFER

The loop filter is composed of C2, R14, C3 which is a pulse forming network, and of R22 and C4 which smooth the pulse derived by C2, R14 and C3. The response of the filter is shown in Figure 4.1. Discussions of the filter appear in Chapters III. and IV.

The output buffer has two functions. First it must isolate the loop filter from any bias currents. This is accomplished by using an FET input op-amp and connecting it

in the non-inverting mode. The second function of the buffer is to shift the resulting error voltage to the center of the VFO operating range. This shifting is done by adding current to the inverting input of the op-amp. This connection forces the output to be a fixed number of volts above or below the normal output voltage independent of the input voltage.

The current providing this offset is supplied by a current mirror formed with Q16. Note that this current mirror is identical to the one described earlier and formed with Q5 except for difference of polarity. Q5 is two NPN transistors instead of PNP transistors. And the emitters of Q5 attach to -15 volts through a resistor instead of +15 volts. To change the polarity of the offset of the output buffer, Q16 can be replaced with a set of NPN transistors, and the +15 volt connection to the emitters can be changed to - 15 volts. As long as the layout provides a way to easily change this voltage connection, output offsets of either polarity can be obtained from the same layout.

E. MINIMIZATION OF CHARGE ACCUMULATION AT THE OUTPUT CURRENT SOURCE

Any stray capacitance at the collectors of Q8 and Q11 will cause a current spike to go into the loop filter when Q12 is switched on. Therefore these lines should be kept short to minimize stray capacitance. Another technique to minimize this spike is to reduce the charge stored in

whatever stray capacitance there happens to be. Transistors Q14 and Q15 along with R18, R19 plus a current source formed with R20, R21, and Q17 comprise a network to keep the voltage at the current source output close to that of the loop filter. Thus when switch Q12 closes, very little charge would transfer into the loop filter.

F. CRITICAL LAYOUT POINTS

Several critical points in the circuit are mentioned here to aid the designer layout a printed circuit board to implement this detector.

1. Current Mirrors

Because the input impedance of the current mirror is low, any stray capacitance from the input to ground will make the current mirror into a very high gain, high frequency amplifier. Any noise between the power supply line and the ground will be amplified by the current mirror. To minimize this noise amplification, the leads should be kept as short as possible.

2. Q1 the C1 Discharge Switch

In order to quickly discharge C1, very short leads are required on Q1 to prevent the discharge current path from disrupting other parts of the circuit and to eliminate distributed inductance which would slow the discharge and cause ringing.

3. Output Current Mirrors

Any stray capacitance at the collectors of Q8 and Q11 will cause a current spike to go into the loop filter when Q12 is switched on. Therefore these lines should be kept short.

4. Switch Drivers

Both the gate and the drain of the switch driver transistors Q4 and Q13 have very large signals on them as compared to the signals driving the VCO. Careful layout of these lines to prevent coupling to other parts of the circuit is essential.

5. Loop Filter

Any signal appearing in the loop filter will cause modulation of the VCO. Therefore precautions should be made when laying out this section of the circuit. In addition to keeping lines short here, a ground shield should encircle all of the connections.

6. VCO Connection

Most varactor tuned microwave oscillators pass the tuning voltage through a mechanical feed thru capacitor. From both a noise standpoint and a driver requirement stand point this feedthrough capacitor should be made a part of the loop filter. R22 and C4 may be thought of in this role. The feedthrough capacitor would replace C4. In other words, C4 would be implemented as a feed through capacitor. And R22 would be attached directly to the feedthrough capacitor.

G. TIMING

The Lock output has a low to high transition when the output goes back into a open circuit state. This signal is delayed slightly by passing it through two NAND gates in U1. It goes through an OR gate (part of the off frequency logic) to a one shot U8b. The one shot generates a 3.33 us. pulse which drives Q13. Q13 generates a +/- 12 volt signal which turns Q12 on and off. At the trailing edged of this pulse, one-shot U8a is triggered. This one-shot generates a 4 us. pulse which drives Q3. Q3 generates a +/- 12 volt signal which turns Q4 on and off. The series connection of the one shots, and the one-shot propagation delay times, insure non-overlapping timing signals.

H. OFF FREQUENCY LOGIC

In the event that either input has no input or is off frequency, the 4046 output will just lock hi or low to drive the system back to the right frequency. When the 4046 output locks up however, no lock pulse is generated. Normally, if no lock pulse is generated, then the output switch will never get closed and the new phase detector would open the loop. To prevent this condition from occurring, U5 and U6 are connected to count the transitions on each input between times that the output switch is closed. If two transitions are made at either input without the output switch getting toggled, then U5 or U6 pass a signal through OR gate U7b to trigger one-shot U8b.

This triggering causes the output switch to close, thus closing the loop. U7a generates a reset pulse to the counters each time the output switch is turned on.

I. POWER SUPPLY

To minimize noise and center the CD4046B output at ground potential, a plus and minus 7 Volt regulator supplies power to the CMOS logic. U9 and U10 are standard positive and negative adjustable regulators. Resistors R28, R29, R30, and R31 were selected to provide 7 volts. Level shifting between the +/- 7 volt logic to the 0/-15 volt one-shot logic is accomplished by D3 and D4.

VI. CIRCUIT PERFORMANCE

Figure 6.1 is an oscilloscope trace of the CD4046 output pulse. The sine wave in this and the other pictures is of the input signal.

Figure 6.2 is an oscilloscope trace of the CD4046 lock-pulse. Notice on the time scale that the low to high transition occurs at the end of the output pulse shown in Figure 6.1.

Figure 6.3 is an oscilloscope trace of the output enable pulse. Comparison with Figure 6.2 shows that it occurs immediately after the output from the CD4046 is finished.

Figure 6.4 is an oscilloscope trace of the charge holding capacitor C1. Note how it ramps up during the time the CD4046 is providing an output, and then it remains constant until the reset pulse occurs.

Figure 6.5 is an oscilloscope trace of the reset pulse. Comparison with Figure 6.3 shows that it occurs immediately after the output enable pulse finishes. Comparison with Figure 6.4 shows that the charge holding capacitor is dumped very quickly after the reset pulse begins.

Figure 6.6 is an oscilloscope trace of the voltage on the loop filter. Ideally it should be a flat line. However, because the test circuit is hand wired with absolutely no shielding, the switch driver signals are coupled into the

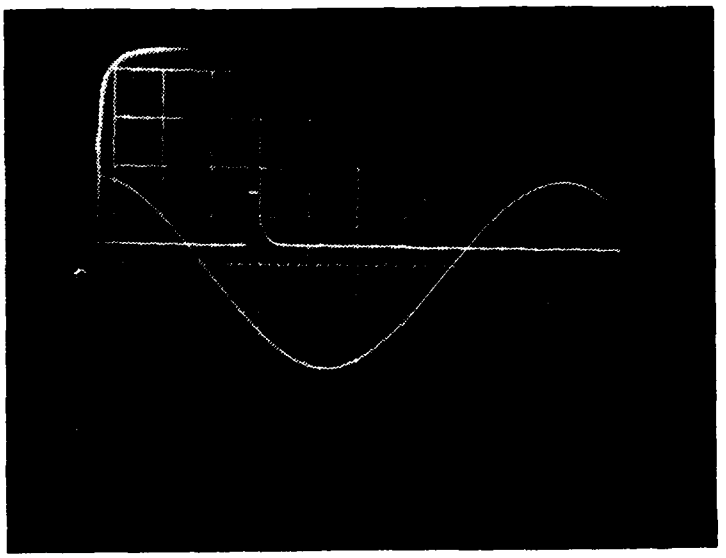


Figure 6.1 Output Pulse From CD4046 (pin 13 of U2)
5V/Div, 60 kHz Input Sine Wave.

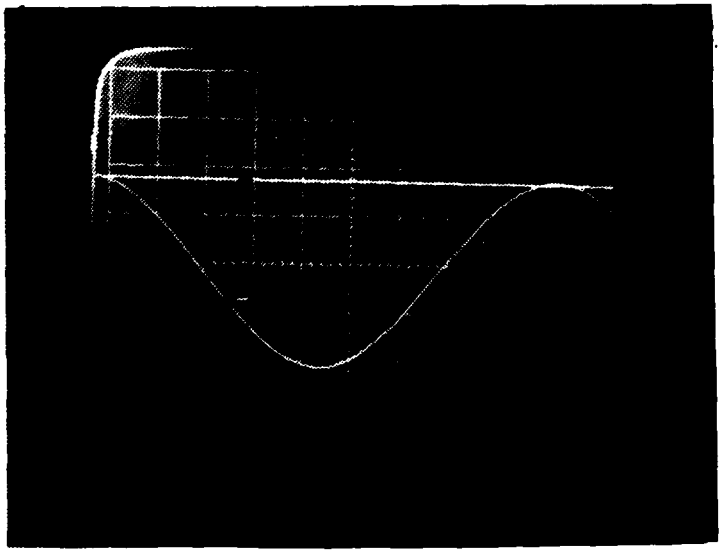


Figure 6.2 Lock Pulse From CD4046 (pin 1 of U2)
5V/Div, 60 kHz Input Sine Wave.

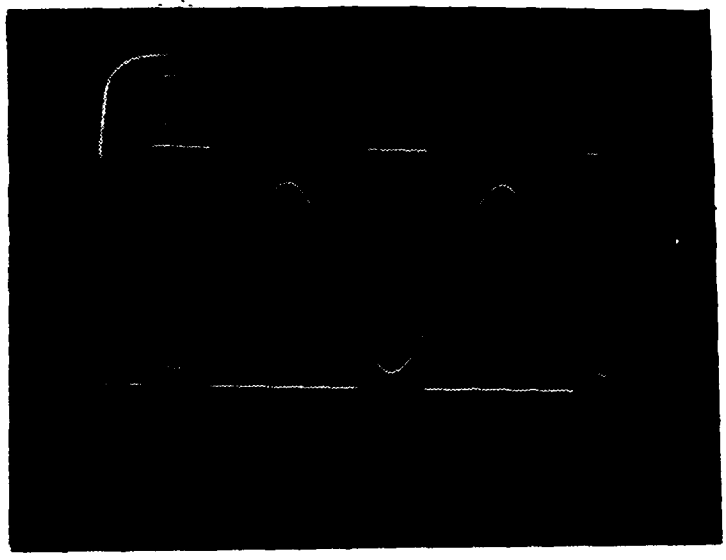


Figure 6.3 Output Enable Pulse (gate of Q12)
5V/Div, 60 kHz Input Sine Wave.

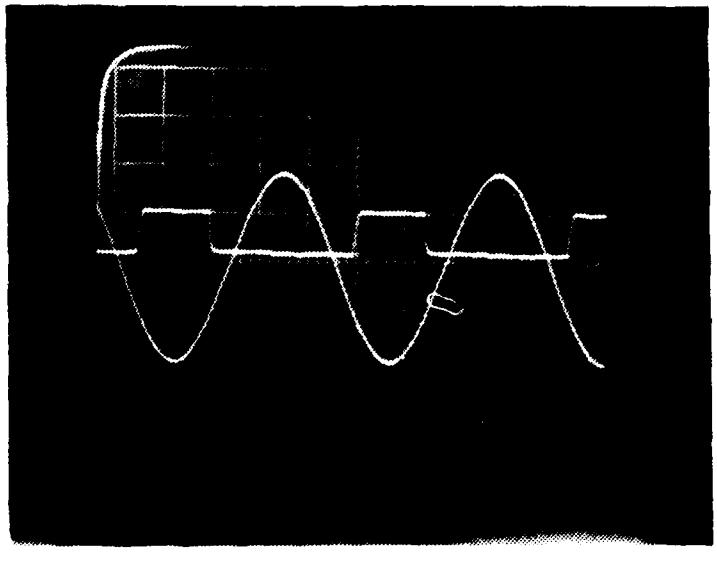


Figure 6.4 Voltage On Charge Holding Capacitor (C1)
100mv/Div, 60 kHz Input Sine Wave.

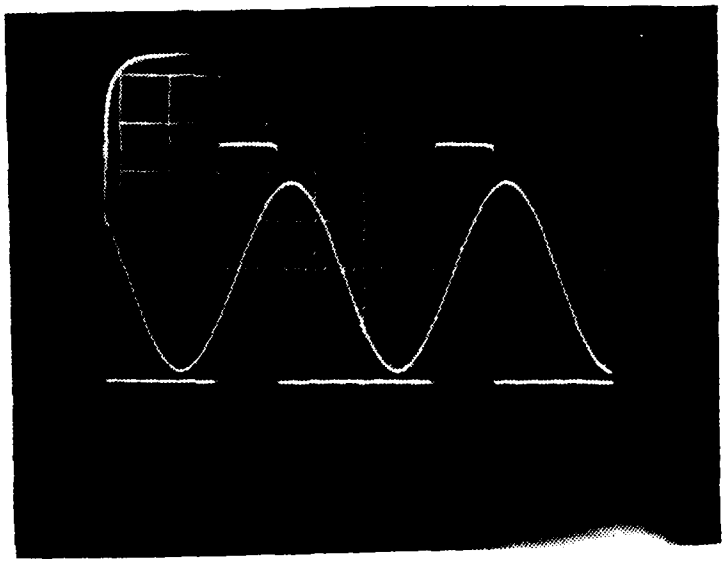


Figure 6.5 Reset Pulse (gate of Q1)
5V/Div, 60 kHz Input Sine Wave

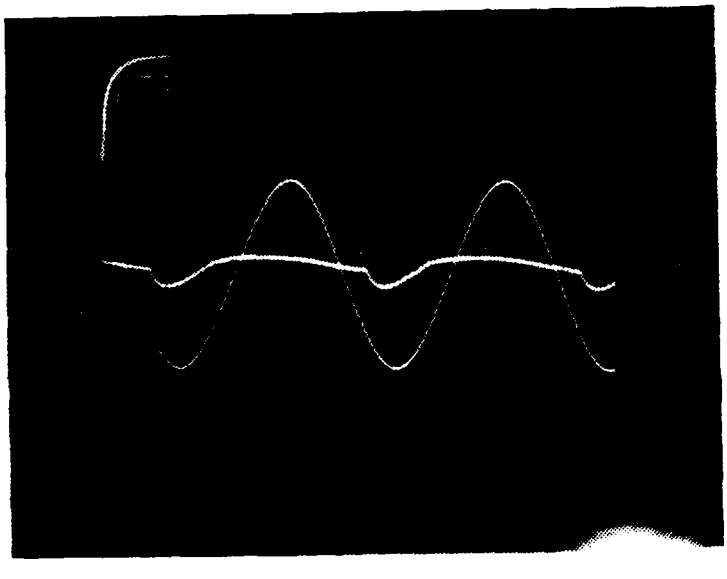


Figure 6.6 Voltage on loop filter (pin 6 of U4)
100mv/Div, 60 kHz Input Sine Wave.

output current source. This problem was predictable since we are looking at millivolt signals with 24 volt driver pulses, no shielding, and a high impedance current source. It does not, however, disrupt the loop to the point where lock-up and successful demonstration of the new phase detector are prevented. The effect of the unwanted coupling is seen in the small voltage dip that occurs in the output during the output enable pulse.

VII. CONCLUSION

A new digital phase detector has been proposed to eliminate the lock-in point dead zone nonlinearity associated with the standard CD4046 type II phase detector. The new digital phase detector was constructed and oscilloscope pictures were made documenting that the proposed detector operated as desired. It has further been shown through computer simulation, that the new detector allows the loop dynamics to be tailored to prevent short, high amplitude control signals while simultaneously providing one cycle settling to frequency changes.

APPENDIX A

COMPUTER SIMULATION MODELS

Figure A1 (a) shows a schematic of the loop filter. The TUTSIM model for the loop filter is shown in block diagram form in Figure A1 (b). The TUTSIM model listing is shown in Figure A2. Table A1 lists the TUTSIM blocks that are used in the simulation models.

Blocks 1, 2, and 3 form a sawtooth generator with a period of 1 sec. Block 5 (relay) models the FET sampling switch. Block 4 provides 0 for zero current. The output of block 15 is current I1. The parameter on Block 5 (relay) determines the duty cycle of selecting 0 or I1. Block 6 is the integration for C2. Block 8 is the integration of current for C3. The rest of the model is self explanatory.

Figure A3 shows a block diagram for the complete phase-locked-loop model. Figure A4 is a listing of the TUTSIM model. The VCO is modeled as an integrator while the reference is modeled with a TIM block. The phase detector becomes just a subtraction. The CD4046 phase detector is modeled with a sample-hold programed for 1 sample per second. The simulation is therefore of a loop locked at a frequency of 1 Hz. Most of the loop is a repeat of the loop filter described previously.

The initial conditions on the loop filter (zero) and VCO (zero) cause the frequency hop condition at t=0. The

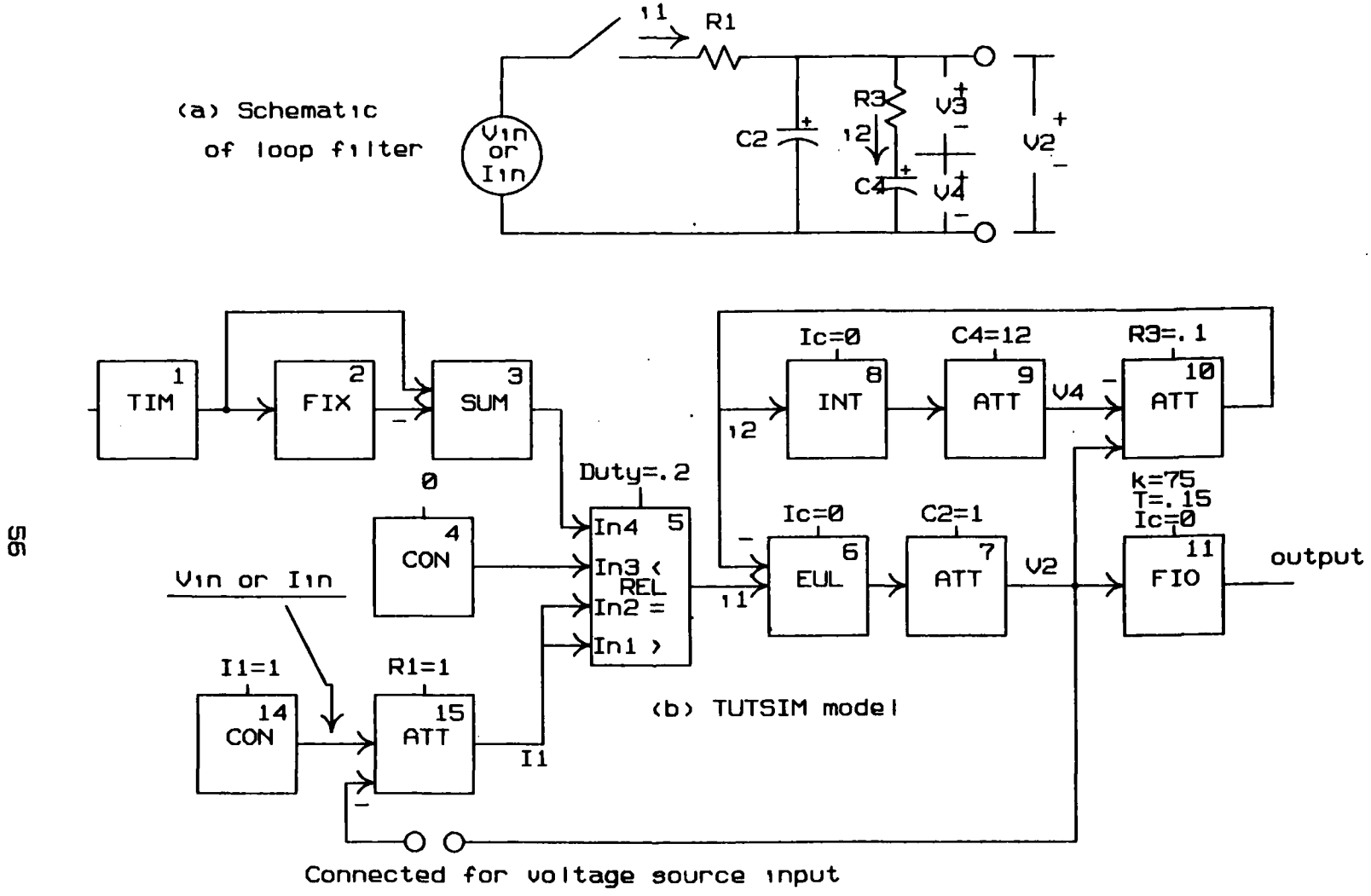


Figure A1. Schematic and Block Diagram of the TUTSIM Loop Filter Model.

```
Model File: filter
Date:      8 /      5 /  1985
Time:     20 :     15
Timing:    0.0050000  ,DELTA  ;    2.0000      ,RANGE
PlotBlocks and Scales:
Format:
     BlockNo,  Plot-MINimum,  Plot-MAXimum;  Comment
Horz:      0 ,    0.0000     ,    2.0000     ; Time
  Y1:      5 ,    0.0000     ,   10.0000     ; Switch Duty Cycle
  Y2:      7 ,    0.0000     ,    0.1000000  ; P=C2 out=V2
  Y3:     11 ,    0.0000     ,    0.1000000  ;
  Y4:        ,               ,               ;

                    1 TIM
                    2 FIX       1
                    3 SUM       1      -2
   0.0000           4 CON                              ;0 input for switch
   0.2000000        5 REL       4       15       15    ;Switch Duty Cycle
                                3
   0.0000           6 EUL       5      -10             ;integeg(i1-i2)
   1.0000           7 ATT       6                      ;P=C2 out=V2
   0.0000           8 INT      10                      ;integeg(i2)
  12.0000           9 ATT       8                      ;P=C4 out=V4
   0.1000000       10 ATT       7       -9             ;P=R3, out=V2-V4=i2
   1.0000          11 FIO       7
   0.1500000
   0.0000
   1.0000          14 CON                              ;input
   1.0000          15 ATT      14                      ;i1
```

Figure A2. Listing of the TUTSIM Loop Filter Model

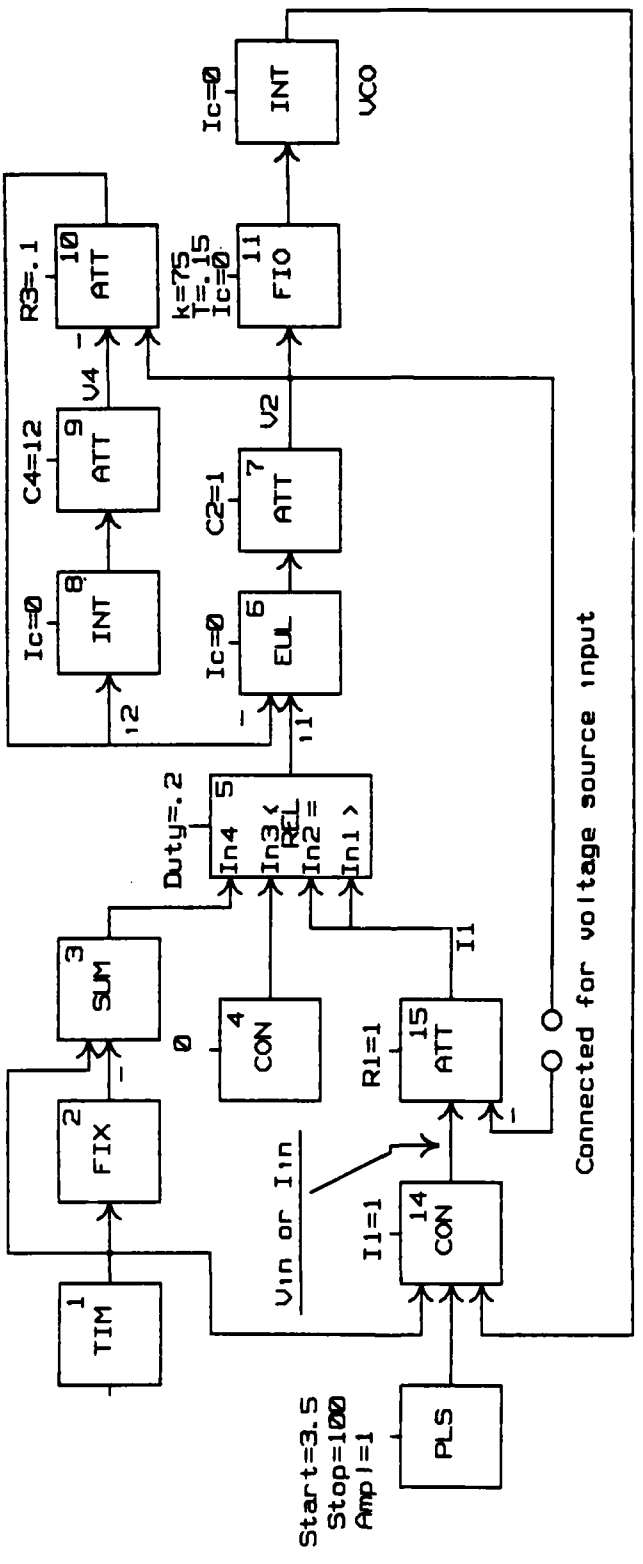


Figure A3. Block Diagram of the TUTSIM PLL Model.

```
Model File: pll
Date:      8 /      5 /  1985
Time:     20 :     14
Timing:    0.0050000   ,DELTA  ;  10.0000      ,RANGE
PlotBlocks and Scales:
Format:
     BlockNo,  Plot-MINimum,  Plot-MAXimum;  Comment
Horz:      0 ,    0.0000     ,   10.0000     ; Time
  Y1:      5 ,   -1.2500     ,    1.2500     ; Switch Duty Cycle
  Y2:     11 ,    0.5000000 ,    1.5000     ; P=K,wRC,Init-Cond
  Y3:        ,              ,               ;
  Y4:        ,              ,               ;

                    1 TIM
                    2 FIX       1
                    3 SUM       1      -2
    0.0000          4 CON                          ;0 input for switch
    0.2000000       5 REL       4       15      15 ;Switch Duty Cycle
                                3
    0.0000          6 EUL       5      -10         ;integ(i1-i2)
    1.0000          7 ATT       6                  ;P=C2 out=V2
    0.0000          8 INT      10                  ;integ(i2)
   13.0000          9 ATT       8                  ;P=C4 out=V4
    0.1000000      10 ATT       7       -9         ;P=R3, out=V2-V4=i2
   70.0000         11 FIO       7                  ;P=K,wRC,Init-Cond
    0.1000000
    0.0000
    0.0000         12 INT      11                  ;VCO
    3.5000         13 PLS
  100.0000
    1.0000
    1.0000         14 SPL       1      13     -12
    1.0000         15 ATT      14                  ;i1
```

Figure A4. Listing of the TUTSIM PLL Model

TABLE A1

BLOCKS USED FROM TUTSIM LIBRARY

TIM - Generates a ramp such that the output equals the time in seconds.

FIX - Converts the sum of its inputs into an Integer.

SUM - Sums its inputs.

REL - Simulates a relay. It has 4 inputs, In1, In2, In3, In4 Input 4 is compared to a programed parameter "P". The output is selected as follows:

out = In1 if In4>P
out = In2 if In4=P
out = In3 if In4<P

ATT - Attenuates the sum of its inputs by the programed parameter.

INT - Integrates the sum of its inputs using a three point Adams-Brashforth method. (best for well behaved inputs). The parameter is the Initial Condition.

EUL - Integrates the sum of its inputs using a two point Euler (trapizoidal) method. (useful when inputs are discontinuous). The parameter is the Initial Condition.

SPL - Sample-Hold samples the sum of its inputs. The period between samples is given with the programed parameter.

CON - Generates a constant output equal to the programed parameter.

PLS - Pulse Generator. Parameters give pulse start time, stop time, and height.

FIO - First-Order filter block generates a $\frac{K}{1 + sT}$ function. K, T, Initial Cond. are the parameters.

loop settles at a frequency of 1 Hz. Block 13 generates a step starting at t=3.5 sec. that is added to the reference. It simulates a phase change that must be corrected.

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Defense Technical Information Center Cameron Station Alexandria, Va. 22304-6145	2
2.	Library, Code 0142 Naval Postgraduate School Monterey, California 93943-5100	2
3.	Professor G. Myers Code 62Mv Department of Electrical Engineering Naval Postgraduate School Monterey, California 93943-5100	5
4.	Commander Naval Surface Weapons Center Attn: Tom Pendergraft Code F40 Dahlgren, Virginia 24062	2
5.	Commander Naval Surface Weapons Center Attn: Mr. Robert Tehlee Code F43 White Oak, Maryland 20910	2
6.	Commander Naval Surface Weapons Center Attn: Library, Code White Oak, Maryland 20910	2
7.	Department Chairman Code 62 Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5100	1
8.	Commander Naval Surface Weapons Center Attn: Mr. John McCorkle Code F43 White Oak, Maryland 20910	12
9.	Professor G. Ewing Code 62Ew Department of Electrical Engineering Naval Postgraduate School Monterey, California 93943-5100	1

END

FILMED

1-86

DTIC